REMARKS

By this Amendment, Applicants amend claims 1-7 to more appropriately define the present invention.

In the Office Action of October 6, 2003, the Examiner objected to the drawings for not showing "the wiring patterns, conductive patterns, and the relative position of the substrate (and substrate features of the through holes and patterns) with respect to the KGD (as in claims 2, 6, and 7) . . . ." *See* Office Action, pg. 2. The Examiner rejected claims 1-7 under 35 U.S.C. § 112, second paragraph "as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." *See* Office Action, pgs. 2-3. The Examiner also rejected claims 1-4 and 6 under 35 U.S.C. § 103(a) as being unpatentable over alleged Applicant admitted prior art and Japanese Patent Heisei 7-211750 (hereinafter, "Nagano"); claims 1-6 under 35 U.S.C. § 103(a) as being unpatentable over alleged Applicant admitted prior art, Nagano, and U.S. Patent No. 6,015,520 (hereinafter, "Appelt"); and claims 1-4 and 6-7 over alleged Applicant admitted prior art, Nagano, and Japanese Patent Publication No. 2000-165047 (hereinafter, "Miura"). See Office Action, pgs. 3-6.

OBJECTIONS TO DRAWINGS

Applicants have amended claims 1-7 to more appropriately define the present invention as well as address the Examiner's objections to the drawings. Accordingly, Applicants respectfully request the Examiner to withdraw the objects to the drawings.

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35 U.S.C. § 112, Second Paragraph

Applicants have amended claims 1-7 to more appropriately define the present invention. Accordingly, Applicants respectfully request the Examiner to withdraw this rejection to claims 1-7.

35 U.S.C. § 103(a)

Applicants respectfully traverse the Examiner's rejection of claims 1-7 under 35 U.S.C. § 103(a) as being obvious. To establish a prima facie case of obviousness, each of three requirements must be met. First, the references, taken alone or combined, must teach or suggest each and every element recited in the claims. (*See* M.P.E.P. § 2143.03 (8th ed. 2001)). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. *See id.* Third, a reasonable expectation of success must exist. *See id.* Moreover, each of the these requirements must "be found in the prior art, and not based on applicant's disclosure." (M.P.E.P. § 2143 (8th ed. 2001)).

Rejection to Claims 1-4 and 6 over Applicant Admitted Prior Art and Nagano

Nagano provides a lead frame having inner leads 4 and a recognition mark metal layer 5 that are covered by a reinforcing tape, so that the back end parts of the inner lead 4 and the recognition mark metal layer 5 are covered while recognition mark 7 (the front part of recognition mark metal layer 5) and the front part of inner leads 4 are exposed. See Nagano, para. 7. Inner leads 4 and recognition mark 7 are on a top surface of a lead frame. See Nagano, Fig. 4. The first layer (or bottom layer) of the

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lead frame is an outer lead 1, for example a 150 micrometer copper foil. Directly on top of outer lead 1, is a middle metal layer 2 which may be 3 to 5 micrometer aluminum. The purpose of middle metal layer 2 is act as an "etching stopper" to prevent etching of inner lead 4 if or when outer lead 1 is etched. See Nagano, para. 9. Contrary to the allegations of the Examiner, the wiring pattern of Nagano is on outer lead 1, not inner lead 4, because the etching takes place on outer lead 1 and inner lead 4 is prevented from any etching. Therefore, recognition mark 5 is not on the same surface as the surface containing the wiring pattern (outer lead 1) and does not disclose "forming wiring patterns on the front surface" and "forming a conductive pattern as a recognition mark on the front surface," as claimed in claim 1.

Applicants' admitted prior art does not overcome the deficiencies of Nagano. As admitted by the Examiner, Applicants' admitted prior art does not disclose that "the recognition mark and the wiring patterns are formed on the same surface (the front surface)." *See* Office Action, pg. 3.

Further, through-hole 6 of Nagano does not extend from a back surface of the lead frame to the front surface. Through-hole 6 of Nagano merely extends through layer 5, as shown in Figure 3 of Nagano. Therefore, because amended claim 1 recites "forming a conductive pattern as a recognition mark on the front surface," Nagano does not disclose the claimed "forming a through-hole from a back surface toward said conductive pattern." *See* amended claim 1. Applicants' admitted prior art does not overcome this deficiency as well, because, as the Examiner admits, Applicants' admitted prior art does not disclose that "the through-hole is formed from the rear surface toward a recognition mark on the front surface." *See* Office Action, pg. 3.

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In addition, the Examiner has provided no motivation to combine the references, nor a reasonable expectation of success. It appears the Examiner is extracting items found in the prior art and combining them without regard to any motivation to combine or a reasonable expectation of success, thereby using Applicants' disclosure as improper hindsight. Such improper hindsight determinations are impermissible under 35 U.S.C. § 103.

Accordingly, Applicants request the Examiner to withdraw this rejection to claim 1. Further, based upon their dependency to allowable independent claim 1, Applicants respectfully request the Examiner to withdraw the rejection to claims 2-5.

Similarly, for the reasons above, Applicants' admitted prior art in view of Nagano does not disclose "forming a conductive pattern as a recognition mark on the front surface; and forming a through hole from the back surface toward said conductive pattern," as claimed in amended claim 6. Accordingly, Applicants respectfully request the Examiner to withdraw this rejection to claim 6.

Rejection to claims 1-6 over Applicant Admitted Prior Art, Nagano, and Appelt

As noted above, the Applicants' admitted prior art and Nagano fail to render obvious claims 1-4 and 6. Appelt fails to overcome their deficiencies.

Appelt discloses a method for filling plated through holes on a printed wiring board. There is no disclosure regarding recognition marks and, accordingly, Appelt fails to disclose "forming a conductive pattern as a recognition mark on the front surface," as claimed in amended claim 1.

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Further, the Examiner has provided no motivation to combine the references, nor a reasonable expectation of success. It appears the Examiner is extracting items found in the prior art and combining them without regard to any motivation to combine or a reasonable expectation of success, thereby using Applicant's disclosure as improper hindsight. Such improper hindsight determinations are impermissible under 35 U.S.C. § 103.

Accordingly, Applicants respectfully request the Examiner to withdraw this rejection to claim 1. Further, claims 2-5 are allowable based, at least, on their dependency upon independent claim 1.

Similarly, for the above reasons, Applet does not overcome the deficiencies of the Applicant admitted prior art and Nagano to render obvious the claim elements of claim 6, including, at least, "forming a conductive pattern as a recognition mark on the front surface; and forming a through hole from the back surface toward said conductive pattern." Accordingly, Applicants respectfully request the Examiner to withdraw this rejection to claim 6.

Rejection to Claims 1-4 and 6-7 Over Applicants' Admitted Prior Art, Nagano, and Miura

As noted above, Applicants' admitted prior art and Nagano fail to render claims 1-4 and 6 obvious. Miura fails to overcome their deficiencies.

Miura discloses a method of manufacturing a printed circuit board that comprises a process of laminating external insulation and conductor layers on the core substrate that has a circuit pattern and a recognition mark. However, in Miura the recognition mark is formed on one internal conductor layer and the Miura through-hole does not

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extend throughout the substrate. There is no disclosure of "forming a conductive pattern as a recognition mark on the front surface; and forming a through hole from a back surface toward said conductive pattern" as claimed in amended claim 1.

Further, the Examiner has provided no motivation to combine the references, nor a reasonable expectation of success. It appears the Examiner is extracting items found in the prior art and combining them without regard to any motivation to combine or a reasonable expectation of success, thereby using Applicants' disclosure as improper hindsight. Such improper hindsight determinations are impermissible under 35 U.S.C. § 103.

Accordingly, Applicants respectfully request the Examiner to withdraw this rejection to claim 1 and claims 2-4, based on their dependency to independent claim 1.

Similarly, for the above reasons, Miura does not overcome the deficiencies of Applicants' admitted prior art and Nagano to render obvious the claim elements of claim 6. Specifically, all the elements of claim 6 are not disclosed, including, at least, "forming a conductive pattern as a recognition mark on the front surface; and forming a through-hole from the back surface toward said conductive pattern." Accordingly, Applicants respectfully request the Examiner to withdraw the rejection to claim 6.

With respect to claim 7, the Examiner admits Applicants' admitted prior art does not disclose "forming wiring patterns on a plurality of layers." Nagano also fails to teach "forming wiring patterns on a plurality of layers." In addition, Applicants' admitted prior art and Nagano fail to teach or suggest "forming the conductive pattern. . .at the same time as forming the wiring patterns," as claimed in amended claim 7.

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Miura fails to overcome the deficiencies of both references. Miura discloses a method of manufacturing a printed circuit board that comprises a process of laminating external insulation and conductor layers on the core substrate, wherein the core substrate has a circuit pattern and a recognition mark formed. *See* Miura, para. 6. Thus, Miura does not disclose forming recognition marks or circuit patterns, it discloses laminating layers of the core substrate which already contains the circuit patterns and recognition marks. There is no disclosure on the formation of the recognition marks. Therefore, Miura does not disclose "forming the conductive pattern. . .at the same time as forming the wiring patterns," as claimed in amended claim 7.

Accordingly, Applicants respectfully request the Examiner to withdraw the rejection of claim 7.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

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Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: December 19, 2003

By: _____
John M. Romary
Reg. No. 26,331

Attachments: Clean Version of Substitute Specification
Marked-Up Version of Substitute Specification.

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SUBSTITUTE SPECIFICATION
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This application is based on Patent Application No. 2001-34324 filed February 9, 2001 in Japan, the content of which is incorporated hereinto by reference.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a method for forming a recognition mark, for performing image recognition, on a substrate as a carrier for an IC socket for inspecting a KGD (Known Good Die, namely, a good bare chip satisfying a specification). More particularly, the invention relates to a method for forming a recognition mark on a substrate in such a manner that the recognition mark can be recognized from a back surface (a surface not formed with a wiring pattern) of the substrate formed with a wiring pattern on one side.

DESCRIPTION OF THE RELATED ART

In the recent years, for higher package density on a circuit board and higher speed, it is becoming typical to surface mount a plurality of bare (namely, before packaging) LSI chips. ~~Associating with~~ From this, it is ~~becoming~~ necessary to inspect the chip by mounting the base chip on an IC socket ~~in the state of the bare chip~~.

~~Upon mounting the chip on the IC socket~~ [[f]]For the purpose of inspection, it is difficult to directly mount the chip on the IC socket. Therefore, a substrate as a bare chip carrier is employed.

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The substrate is formed by forming a conductive wiring (wiring pattern) of copper or the like on a film form insulating substrate of polyimide or the like, namely, on a flexible insulating substrate. The wiring pattern is formed on the insulating substrate in such a manner that a conductive layer, which is formed by bonding of a conductive foil or plating, is processed to establish a predetermined wiring pattern by etching or the like.

On the substrate as set forth above, a recognition mark for performing image recognition or other processes depending upon application thereof is provided. The recognition mark is typically formed at the same time [[of]] as formation of the wiring pattern with the conductive layer forming the wiring pattern.

However, in the flexible substrate, a bump can be formed on the back surface (the surface ~~not formed~~ where the wiring pattern is not formed) for the purpose of electrical connection with the bare chip as exemplarily illustrated in Figs. 5A and 5B. In the bump forming process shown in Figs. 5A and 5B, the bump 4 is formed through the following processes. (1) At portions to form the bumps 4, holes 3 are formed in the insulating substrate 1 by laser machining from the back surface 5 of the insulating substrate where the conductive pattern is not formed (*see* Fig. 5A). (2) Subsequently, with resisting and plating on the insulating substrate 1, plating is selectively grown only in the portions where the holes 3 are formed to form the bumps 4 (*see* Fig. 5B).

As set forth above, in the substrate formed with the bumps on the back surface, the bare chip to be inspected is naturally mounted on the back surface of

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the substrate. Therefore, it is required for the recognition mark to be provided on the back surface of the substrate.

As a conventional method for forming the recognition mark on the back surface of the substrate, the following processes have been considered, for example:

(1) a method using an insulating substrate 1 having conductive layers on both surfaces, wherein the recognition mark 6 is formed by etching the conductive layer on the back surface 5 in similar process to formation of the wiring pattern 2 (see Figs. 6A and 6B); and

(2) a method for forming the insulating substrate of a transparent material, and then forming the recognition mark 6 together with the wiring pattern (see Figs. 7A and 7B).

However, in case of the substrate formed with the recognition mark by the method of (1), while no problems will be encountered in ~~use of~~ using the substrate for inspecting the chip, the conductive layers are required on both surfaces of the insulating substrate[[,]]. [[and]] Also, two etching steps, for the front surface and the back surface, are required in a fabrication process[[,]]. [[t]]Thereby inherently ~~causing rising~~ raising of manufacturing costs.

In case of the substrate formed with the recognition mark by the method of (2), while no problems will be encountered as long as the insulating substrate ~~being~~ is kept transparent, the insulating substrate may be tarnished by being exposed in a high temperature atmosphere resulting in ~~causing difficulty~~ difficulties in recognition. Particularly, ~~in inspection of~~ when inspecting the KGD, since the substrate has to be

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exposed in a high temperature atmosphere for a long period, [[such]] the substrate is not suitable for repeated use as the KGD carrier.

SUMMARY OF THE INVENTION

The present invention has been worked out for solving the drawbacks in the prior art set forth above. Therefore, it is an object of the present invention to provide a method for forming a recognition mark on a back surface of a substrate which can be fabricated in reduced manufacturing cost, is easy to manufacture and permits repeated use of the substrate formed with the recognition mark.

In order to achieve the above object of the present invention, a method for forming a recognition mark on a substrate for a KGD, wherein wiring patterns are formed on a surface of one side of an insulating substrate, is featured [[in]] as comprising the following steps. The first step is forming a conductive pattern as a recognition mark on one surface where the wiring patterns are formed. The second step is forming a through hole from a surface where the wiring pattern is not formed toward the conductive pattern.

In a method for forming a recognition mark on a substrate for a KGD, the substrate is formed with a bump to be connected to the KGD on the surface where the wiring pattern is not formed.

In a method for forming a recognition mark on a substrate for a KGD, the conductive pattern may also have a particular shape as the recognition mark. Alternatively, in a method for forming a recognition mark on a substrate for a KGD, a shape of the through hole may define the recognition mark.

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Further, a method for forming a recognition mark on a substrate for a KGD can be applied to the substrate that wiring patterns are formed on a plurality of layers of an insulating substrate.

The above and other objects, effects, features and advantages of the present invention will become more apparent from the following description of embodiments thereof taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a plan view for explaining the first embodiment of a method for forming a recognition mark according to the present invention;

Fig. 1B is a sectional view taken along line IB-IB of Fig. 1A;

Fig. 2A is a plan view for explaining the second embodiment of a method for forming a recognition mark according to the present invention;

Fig. 2B is a sectional view taken along line IIB-IIB of Fig. 2A;

Fig. 3A is a plan view for explaining the third embodiment of a method for forming a recognition mark according to the present invention;

Fig. 3B is a sectional view taken along line IIIB-IIIB of Fig. 3A;

Fig. 3C is showing variations of combination of conductive patterns and through holes;

Figs. 4A to 4C show applications of the method for forming the recognition mark according to the present invention, in which Fig. 4A is an application to the substrate having wiring on both surfaces, Fig. 4B is an application to the substrate for multi-layer interconnection boards, and Fig. 4C is an application to another substrate for multi-layer interconnection boards;

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Figs. 5A and 5B are sectional views showing prior art in forming bumps in the substrate;

Fig. 6A is a plan view for explaining the first prior art of a method for forming a recognition mark ~~according to the present invention~~;

Fig. 6B is a section taken along line VIB-VIB of Fig. 6A;

Fig. 7A is a plan view for explaining the second prior art of a method for forming a recognition mark ~~according to the present invention~~; and

Fig. 7B is a sectional view taken along line VIIB-VIIB of Fig. 7A.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

(First Embodiment)

Figs. 1A and 1B show a substrate for explaining the first embodiment of a method for forming a recognition mark according to the present invention.

In the method shown in Figs. 1A and 1B, a conductive pattern 7 (in the shown embodiment, substantially square conductive pattern) is preliminarily formed on one side (a front surface) of an insulating substrate 1, on which a wiring pattern is to be formed. Then, a through hole 8 of an predetermined shape (in the shown embodiment, cross shape) as a recognition mark is formed at a suitable position (in the shown embodiment, substantially center position of the substrate) corresponding to a portion where the conductive pattern 7 is formed, by laser machining from a back surface 5 of the insulating substrate 1. Accordingly, in the shown embodiment, the cross-shape through hole 8 per se or the conductive pattern 7 appeared as cross-shape from the back surface is considered as the recognition mark.

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It should be understood that the conductive pattern 7 to be formed in the shown embodiment can be formed simultaneously with formation of the wiring pattern by etching or the like. It should be also understood that the cross shape through hole 8 can be formed by laser machining simultaneously with formation of holes for bumps.

The shapes of the conductive pattern 7 and the through hole 8 should not be limited respectively to the square shape and the cross shape. Namely, the shape of the conductive pattern 7 may be a simple shape, such as circular shape, quadrangular shape and so on, and the shape of the through hole 8 may be any particular shape as the recognition mark to be formed within the area of the conductive pattern 7. Thus, both shapes may be any arbitrarily selected shapes. Furthermore, ~~as a matter obvious,~~ both are formed at positions other than the positions of the bumps.

As set forth above, with the shown embodiment of the method for forming the recognition mark, the recognition mark can be easily formed on the back surface of the substrate without adding a special manufacturing step.

(Second Embodiment)

Figs. 2A and 2B show a substrate for explaining the second embodiment of a method for forming the recognition mark according to the present invention.

In the method shown in Figs. 2A and 2B, the through hole 8 formed by the method of the first embodiment, is filled with plating 9 or the like to be flush with the back surface, so that the cross-shaped plating 9 is considered as the recognition mark in the shown embodiment. It should be noted that plating is a preferred

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material to fill the hole, so that the recognition mark may be formed simultaneously with formation of bumps. However, the material to fill the hole is not necessarily the plating as in the shown embodiment, but can be any suitable material[[s]]. For instance, a material of a color different from the color of the insulating substrate may be used.

Even in the method of the shown embodiment, the recognition mark can be easily formed on the back surface of the substrate without adding any additional manufacturing steps. Furthermore, since the recognition mark is formed [[in]] flush with the back surface, focusing on the recognition mark is facilitated.

(Third Embodiment)

Figs. 3A and 3B show a substrate for explaining the third embodiment of a method for forming the recognition mark according to the present invention.

In the method shown in Figs. 3A and 3B, the shapes of the conductive pattern 7 and the through hole 8 are reversed from the shapes in the first embodiment. Namely, the shape of the through hole 8 is simple shape, such as circular shape, quadrangular shape or the like and the shape of the conductive pattern 7 is a particular shape as the recognition mark formed within the area of the through hole 8.

As a concrete method for formation, in a similar manner as the first embodiment, a conductive pattern 7 (in the shown embodiment, the conductive pattern, in which substantially cross-shaped punched hole 10 is formed) is preliminarily formed on one side (a front surface) of an insulating substrate 1, on which a wiring pattern is to be formed. Then, a through hole 8 of an predetermined

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shape (in the shown embodiment, circular shape) is formed at a suitable position (in the shown embodiment, substantially center position of the substrate) corresponding to a portion where the conductive pattern 7 is formed, by laser machining from a back surface 5 of the insulating substrate 1. In the shown embodiment, the cross shape punched hole 10 is taken as the recognition mark to be recognized from the back surface side.

The shape of the recognition mark is not limited to the cross-shaped punched hole 10 as in the shown embodiment but can be any particular shape recognizable as the recognition mark in the through hole 8. For example, any shapes as shown in Fig. 3C may be employed. As the case may be, a part of the wiring pattern may be used as the recognition mark.

Even in the shown embodiment, the recognition mark can be easily formed on the back surface of the substrate without adding any additional manufacturing steps. Furthermore, since the through hole in simple shape is required to be formed[[,]] so that a particular shape as the recognition mark can be recognized, particular precision is not required in forming the through-hole.

(Other Embodiment)

In Figs. 4A to 4C, several examples of application of the first embodiment of the method for forming the recognition mark will be explained.

In an application shown in Fig. 4A, a substrate is formed with wiring pattern 2 on both surfaces of the insulating substrate 1. In this case, together with the wiring pattern on the surface not connected to the chip, the conductive pattern 6 as the recognition mark is formed so as to be visible through the through hole 8.

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In applications shown in Figs. 4B and 4C, a substrate is formed with wiring patterns in multiple layers. In these cases, the conductive layer 6 as the recognition mark is formed together with the wiring pattern in arbitrary layer other than the layer connected to the chip, e.g. the lowermost layer in case of Fig. 4B and second layer in case of Fig. 4C.

As set forth above, with the method for forming the recognition mark according to the present invention, the recognition mark can be formed in the arbitrary layer in the substrate of the multiple layer structure to increase freedom in designing and forming of the wiring pattern.

As set forth above, since the method for forming the recognition mark on the back surface of the substrate for KGD inspection socket is adapted for the substrate having the wiring pattern formed on one surface of the insulating substrate, forms the conductive pattern as the recognition mark on one surface where the wiring pattern is formed, and forms a through hole from the surface where the wiring pattern is not formed, toward the conductive pattern, the recognition pattern can be easily formed on the back surface of the substrate without requiring any additional ~~of particular~~ process steps. As a result, it becomes possible to provide a substrate which can be used repeatedly and is inexpensive.

The present invention has been described in detail with respect to preferred embodiments, and it will now be apparent from the foregoing to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspect, and it is the intention, therefore, in the apparent

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claims to cover all such changes and modifications as fall within the true spirit of the invention.

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ABSTRACT OF THE DISCLOSURE

A method for forming a recognition mark on the back surface of a substrate for a KGD that can be easily produced ~~while manufacturing cost is low~~ at a low manufacturing cost and permits repeated use of a substrate is provided. In the method, wiring patterns are formed on a surface of one side of an insulating substrate. The method includes a step of forming a conductive pattern as a recognition mark on one surface where the wiring patterns are formed, and a step of forming a through hole from a surface where the wiring pattern is not formed toward the conductive pattern. In the substrate, bumps connected with the KGD are formed on the surface on which the wiring patterns are not formed. Also, the conductive pattern may have a shape as the recognition mark or the through hole may have the shape as the recognition mark.

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